

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claim 1 (cancelled)

2. (Currently Amended) ~~The~~ A nonvolatile semiconductor memory device ~~according to claim 1,~~ comprising:

a source region and a drain region that are disposed on a main surface of a semiconductor substrate and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above said channel region on a side toward said drain region and via a first gate dielectric film; and

a second gate that is provided above said channel region on a side toward said source region via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film;

wherein said first gate is formed so as to cover said first gate dielectric film, a lateral surface of said first dielectric film, and a lateral surface of said second

dielectric film;

wherein one end of said first gate is positioned on an upper end face of said second dielectric film; and

wherein said first gate is positioned with both ends placed in a gap region enclosed by said second gate and is filled so as to form a concave portion.

3. (Currently Amended) ~~The~~ A nonvolatile semiconductor memory device ~~according to claim 1,~~ comprising:

a source region and a drain region that are disposed on a main surface of a semiconductor substrate and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above a channel region on a side toward said drain region and via a first gate dielectric film, and

a second gate that is provided above a channel region on a side toward said source region via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film;

wherein said first gate is formed so as to cover said first gate dielectric film, a lateral surface of said first

dielectric film, and a lateral surface of said second dielectric film;

wherein one end of said first gate is positioned on an upper end face of said second dielectric film; and

wherein ~~the~~ a surface area of said first gate is $A > B + C + D$ when ~~the~~ a sidewall area within a gap region of said second gate is A, ~~the~~ a bottom surface area within a the gap region of said second gate is B, ~~the~~ a flat surface area of ~~the~~ a top of said second gate is C, and ~~the~~ a sidewall area of the top of said second gate is D.

4. (Currently Amended) The nonvolatile semiconductor memory device according to claim ~~12~~, wherein said second gate controls said channel region on a side toward said source region ~~a split channel formed within said semiconductor substrate via said second gate dielectric film.~~

5. (Currently Amended) The nonvolatile semiconductor memory device according to claim ~~14~~, wherein said second gate has a gate function as ~~for controlling both an erase gate and a split channel and acting as erase gate.~~

6. (Currently Amended) The nonvolatile semiconductor memory device according to claim ~~12~~, wherein said second gate dielectric film is the same as a gate dielectric film

for a MOS transistor ~~that composes for~~ a low-voltage section of a peripheral circuit formed on said semiconductor substrate.

7. (Currently Amended) The nonvolatile semiconductor memory device according to claim ~~12~~, wherein ~~the~~ a material and film thickness of said second gate are the same as those of a gate for a MOS transistor ~~that composes for~~ a peripheral circuit formed on said semiconductor substrate.

8. (Currently Amended) A nonvolatile semiconductor memory device, comprising:

a source region and a drain region that are ~~mounted~~ disposed on a main surface of a semiconductor substrate and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above said ~~a~~ channel region on a side toward said drain region and via a first gate dielectric film;

a second gate that is provided above said ~~a~~ channel region on a side toward said source region via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film;

a third gate that is provided via a third dielectric film formed on said first gate;

a word line that is electrically connected to said third gate;

a contact hole ~~that is made through a third dielectric film formed on said~~ word line ~~third gate~~; and

metal wiring that is connected to said word line via said contact hole;

wherein said contact hole is provided above ~~on~~ a member having the same material and film thickness as a film that forms said second gate.

9. (Original) The nonvolatile semiconductor memory device according to claim 8, wherein said member is a polysilicon film.

Claim 10 (Cancelled)

11. (Currently Amended) ~~The~~ A nonvolatile semiconductor memory device, comprising:

a well of a first conductivity type that is formed on a main surface of a semiconductor substrate;

a source region and a drain region that are formed in said well and positioned at a specified distance from each other;

a channel region that is formed between said source region and said drain region;

a first gate that is provided above said channel region on a side toward said drain region and via a first gate dielectric film;

a second gate that is provided above said channel region on a side toward said source region via a second gate dielectric film, wherein a lateral surface of said second gate is covered with a first dielectric film and an upper surface of said second gate is provided with a second dielectric film; and

a third gate that is provided via a third dielectric film formed on said first gate;

wherein a bind region for binding a plurality of said second gates is provided on a region of said semiconductor substrate where an impurity diffusion layer including a second conductivity type is selectively formed, and

~~according to claim 10,~~ wherein said an impurity diffusion layer region including said second conductivity type is connected to said source region, said drain region, and a diffusion layer region of a select transistor for selecting said source region and drain region.

Claims 12-16 (Cancelled)

17. (New) The nonvolatile semiconductor memory device according to claim 3, wherein said second gate controls said channel region on a side toward said source region via said second gate dielectric film.

18. (New) The nonvolatile semiconductor memory device according to claim 17, wherein said second gate has a function as an erase gate.

19. (New) The nonvolatile semiconductor memory device according to claim 3, wherein said second gate dielectric film is the same as a gate dielectric film for a MOS transistor for a low-voltage section of a peripheral circuit formed on said semiconductor substrate.

20. (New) The nonvolatile semiconductor memory device according to claim 3, wherein the material and film thickness of said second gate are the same as those of a

gate for a MOS transistor for a peripheral circuit formed on said semiconductor substrate.